SIMULATION OF AN INTEGRATED INTER-DIGITAL CAPACITOR WITH SUBSTRATE FOR BUCK CONVERTER

Abdelhadi Namoune[1*],and Rachid Taleb[2]

[1]*Electrical Engineering Department, Ahmed Zabana University Center, Relizane, Algeria*
[2] *Electrical Engineering and Renewable Energies Laboratory (LGEER) Hassiba Benbouali University, Chlef, Algeria*

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Abstract-The on-chip radio frequency (RF) capacitor is one of the key components for RF integrated circuit designs such as filters and converters. This paper presents the physical model and equivalent lumped circuit of an inter-digital capacitor is first determined. Quality factor is the essential parameter as it is an index for the efficiency of a capacitors performance. Moreover, the results of different simulations concern the effects of geometrical parameter variations on capacitance value and quality factor are shown and discussed. Finely, we achieved simulations on the operating of our buck converter including firstly a classical capacitor, secondly an integrated inter-digital capacitor. Simulation results have shown that the waveforms of the output current and voltage in both cases are similar.

Keywords— Inter-digital capacitor, Integrated circuit, Radio frequency, Buck converter, Substrate.

1. Introduction

The always-augmenting demand for multifunctional and undersize portable electronic devices is driving the improvement of miniaturized DC-DC converters [1 – 3]. Such converters are used to shift voltage levels in electronic systems with high efficiency. There are multiple applications for such converters. For example, state-of-the-art portable smart phones and tablet PCs feature multiple components, such as the display panel, MEMS sensors, data storage devices, and cameras, which may require different operating voltage levels. Miniaturizing these converters reduces the overall size of the portable devices [4].

Passive components are the major factor in determining the overall size, cost and performance of portable products. The drive to further miniaturization and integration of portable electronic devices has recently focused on the task of passive functions [5, 6].

Integration of passive devices in the same silicon substrate is desirable in order to reduce this interconnect parasitic, reduce the size and cost of the units and increase the operating frequencies of the radio frequency circuits. Capacitors are elementary and important parts in radio frequency circuits [7].

In this paper, the behavior of inter-digital capacitor is systematically studied and the impact of the geometrical parameters on its capacitance and quality factor. The principal object of my paper is to detail all the phases of design and modeling of an inter-digital capacitor in order to attain its simulation and integrate it into a buck converter. This structure increases the quality factor value while reducing the constituent dimensions with a small manufacturing cost.

2. DC-DC Buck converter

The buck converter circuit is shown in figure 1. The switch T has a duty cycle D which ranges from 0 to 1. Figure 2 indicates relevant waveforms of the circuit when the switch T is turned ON and OFF at frequency f, with a duty cycle D.

*Corresponding author: *E-mail:* namoune.abdelhadi@gmail.com

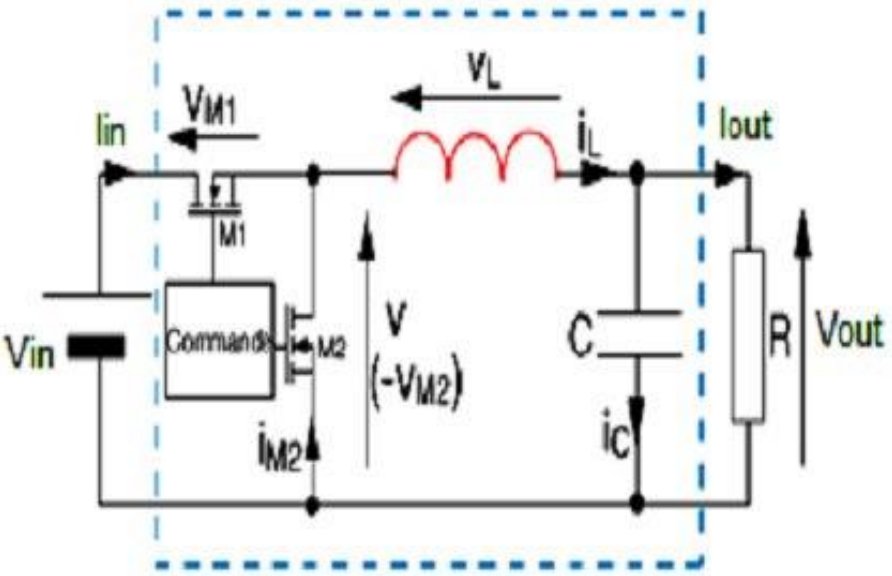

Figure 1 Schematic of a typical DC-DC buck converter

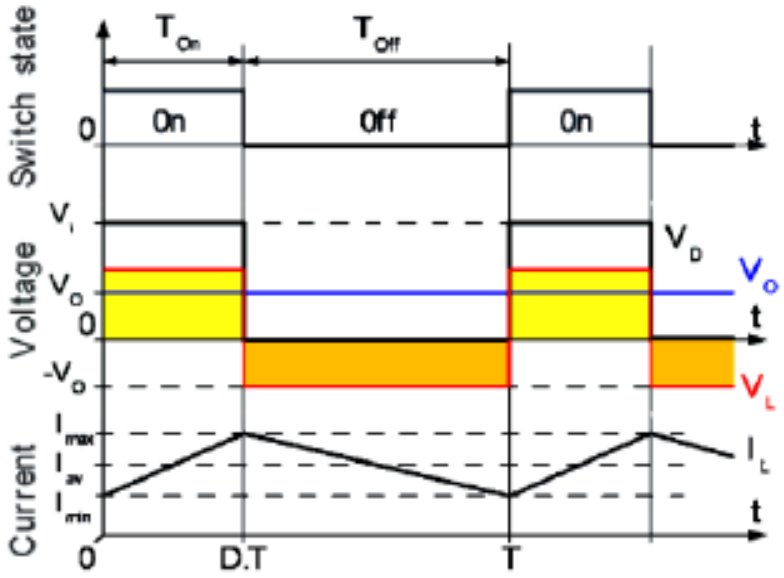

Figure 2 Waveforms of the voltages and currents with time in a buck converter

The following equations then hold for the buck converter.

$$I_{out} = \frac{P_{out}}{V_{out}} \quad (1)$$

$$D = \frac{V_{out}}{V_{in}} \quad (2)$$

$$L = \frac{(V_{in} - V_{out}).D}{2.\Delta I_L.f} \quad (3)$$

The design specifications of buck converter with an output power of 0.6 w are enlisted in Table I:

Table 1: Material Specification

Elements	Material	Characteristics
Conductor	Copper (Cu)	Resistivity : $\rho_{Cu} = 1.7 \times 10^{-8}$ [Ω.m] Conductivity : $\sigma_{Cu} = 5.8 \times 10^{7}$ [S/m]
Oxide	Silicon dioxide (SiO_2)	permittivity : $\varepsilon_{ox} = 3.97\ \varepsilon_0$ $\varepsilon_0 = 8.85 \times 10^{-12}$ [F/m]
Substrate	Silicon (Si)	Resistivity : $\rho_{Si} = 2.27 \times 10^{-1}$ [Ω.m] Permittivity : $\varepsilon_{Si} = 11.9\ \varepsilon_0$

1. Design and modeling inter-digital capacitor

Inter-digital capacitors have proven to be useful components in radio frequency integrated circuits (RFIC) due to their simplicity of construction. Their use afford a considerable size reduction when compared with equivalent distributed matching structures and they are higher yield, lower loss and more repeatable than overlay capacitor [8].

Fig. 3 shows a 3D view a typical inter-digital capacitor with five fingers. The geometry design variables for an inter-digital capacitor are n is the number of fingers, l is the finger length, w is the finger width, s is the spacing between fingers, g is the gap width at the end of each finger, t is the metallization thickness, h is the substrate height, and εr is the dielectric constant.

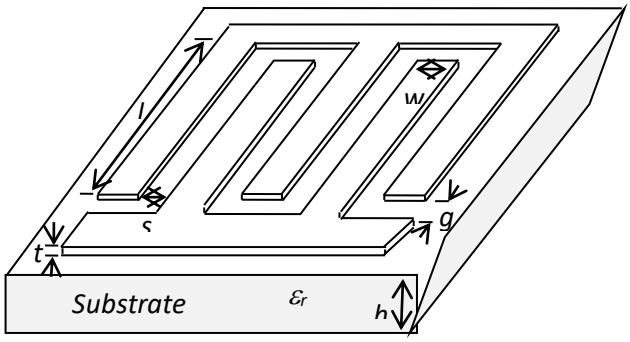

Figure 3 Transverse section of an inter-digital capacitor with five fingers placed on the substrate.

The inter-digital capacitor parameters are summarized in *Table 2*

Table 2: Parameter value for the inter –digital capacitor

Parameter	Symbol	Values
Number of finger	n	5
Finger length	l	210 µm
Finger width	w	38 µm
Spacing between fingers	s	25 µm
Gap width at the end of each finger	g	10 µm
Metallization thickness	t	5 µm
Substrate height	h	400 µm
Substrate dielectric constant	ε_r	2,4

An exact study approved by [9, 10] established the lamped circuit equivalent of an Inter-digital capacitor which is shown in Fig. 4.

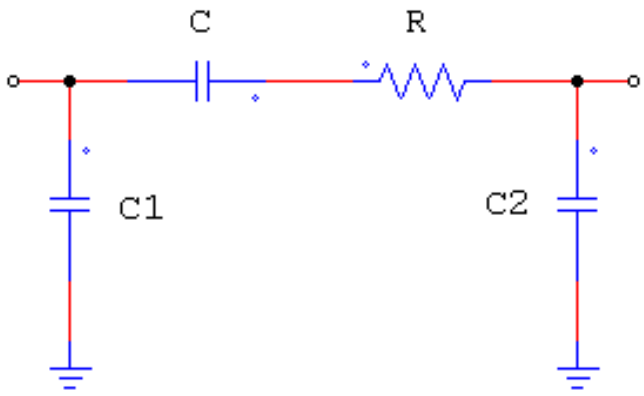

Figure 4 Equivalent circuit model of the inter-digital capacitor

In this model, the series capacitor C accounts for the capacitance between the fingers, whereas the series resistance R resulting from a finite conductivity of metallic components of the element. The capacitance C1 and C2 are given by scattering capacitance with respect to the earthling metallization and their magnitude decreases with increasing substrate thickness.
The series resistance R of an inter-digital capacitor increases with frequency due to skin effect resistance, can be expressed by [11]:

$$R = \frac{4R_s l}{3w} \tag{4}$$

Where, R_s is surface resistivity or skin effect resistance and can be described as follows [12]

$$R_s = \sqrt{\rho \pi \mu_0 f} \tag{5}$$

The series capacitor C is the most important element [13] presented the following expressions

$$C = \frac{\varepsilon_{eff}.10^{-8}.K(k)}{18.\pi.K'(k)}(n-1).l \quad (6)$$

Where, the ratio of complete elliptic integral of first kind K(k) and its complement K'(k) is given by [14]:

$$\frac{K(k)}{K'(k)} = \begin{cases} \frac{\frac{1}{\pi}ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right)}{\pi} for\ 0{,}707 \le k \le 1 \\ \frac{}{ln\left[2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right]} for\ 0 \le k \le 0{,}707 \end{cases} \quad (7)$$

$$k = tan\left(\frac{w.\pi}{4(w+s)}\right)^2 \quad (8)$$

$$k' = \sqrt{1-k^2} \quad (9)$$

The capacitors C1 and C2 are approximately calculated on the basis that for s/h << 1, magnetic field lines do not loop around each finger but around the cross section of the inter-digital width. The C1 is calculated using micro strip transmission theory.

$$C1 = C2 = \frac{0{,}5.l.\sqrt{\varepsilon_{eff}}}{150.10^8} \quad (10)$$

Where, ε_{eff} is the effective dielectric constant.

The Table III gives the results of technological parameters of the integrated inter-digital capacitorIn this model, the series capacitor C accounts for the capacitance between the fingers, whereas the series resistance R resulting from a finite conductivity of metallic components of the element. The capacitance C1 and C2 are given by scattering capacitance with respect to the earthing metallization and their magnitude decreases with increasing substrate thickness

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Table 3: Electrical parameters of the integrated capacitor

Electricals parameters	Symbol	Values
Series capacitor	C	55 fF
Parasitic capacitances	C1,C2	10 fF
Series resistor	R	0,884 mΩ

The performance parameters capacitance and quality factor can be directly computed from the inter-digital capacitor Y-parameters as [15]:

$$C = 2\pi f.Im\frac{1}{Y_{21}} \quad (11)$$

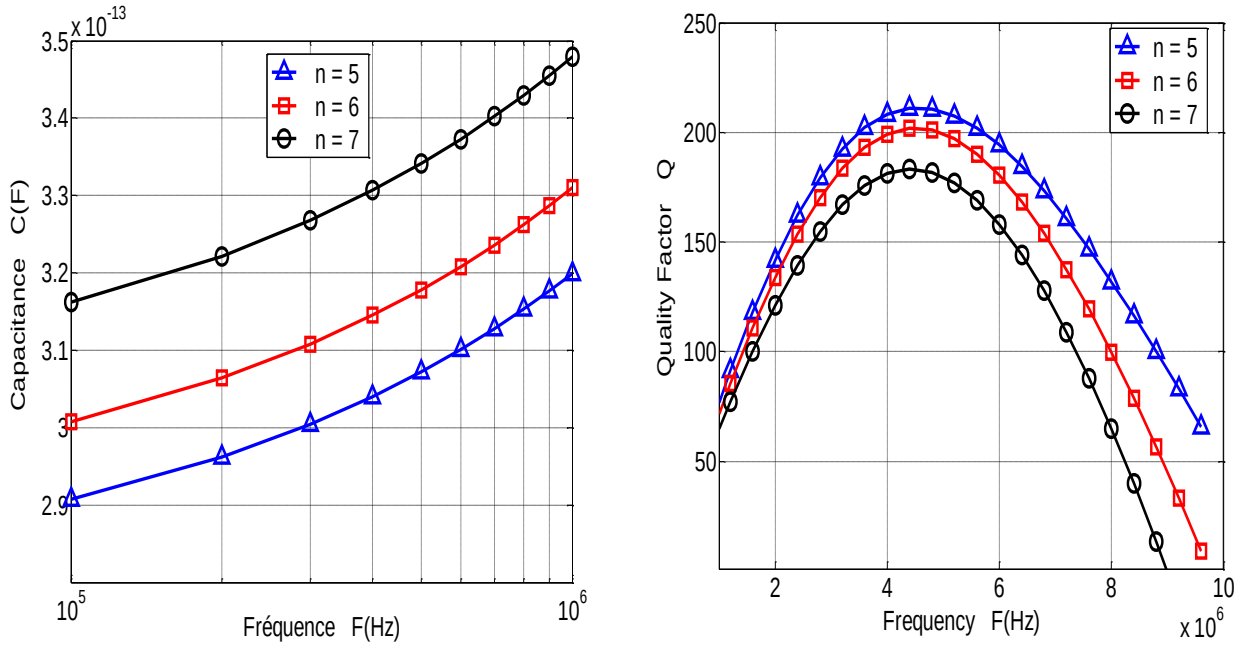
$$Q = \left|\frac{Im(Y_{11})}{Re(Y_{11})}\right| \quad (12)$$

2. Results and discussions

The inter-digital capacitor has been simulated in the frequency range of 1 MHz to 10 MHz by varying the parameters such as the number of finger, spacing between fingers, finger length and finger width while maintaining a fixed area of the structure. The results using geometric parameters give some insights on the simulated results obtained from the MATLAB software

2.1.Influence of the number of fingers

Number of fingers gives huge impact to the inter-digital capacitor performance. The capacitance value increases with increasing number of fingers. However, the quality factor value is inversely proportional to the number of fingers. As shown in Fig. 5(a), the capacitance curves increase when number of fingers increases from 5 to 7. Fig. 5(b) shows that when the number of fingers increases, the quality factor decreases.



a b

Figure 5 Influence of the number of fingers on the capacitance and quality factor of the inter-digital capacitor. (a) Capacitance as a function of frequency; (b) quality factor as a function of frequency

2.2.Influence of the spacing between fingers

The plots in Fig. 6(a) and Fig. 6(b) illustrate the effect of varying the spacing between fingers on the capacitance and quality factor. It can be observed that increasing the space between fingers results in a higher capacitance value and a lower quality factor.

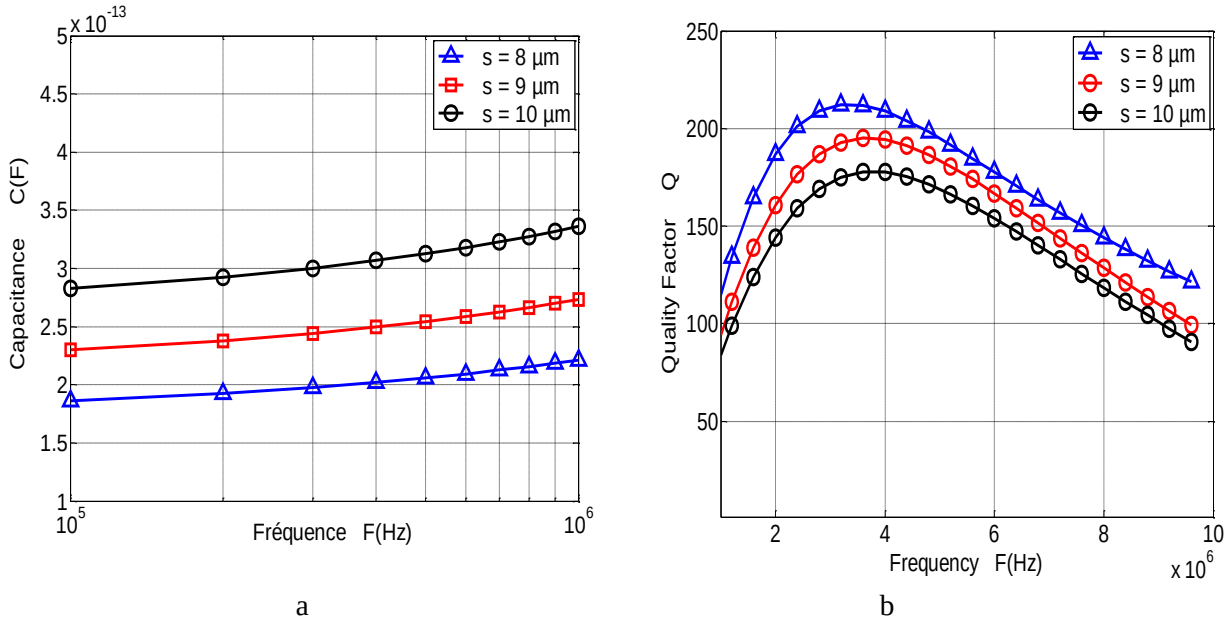


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Figure 6 Simulation results for (a) Capacitance, (b) Quality factor by varying the spacing between fingers

2.3.Influence of the finger length

The effects of finger length on capacitance and quality factor were simulated. As shown in Fig. 7(a), obviously the capacitance, C value increases when finger length increases from 200 µm to 280 µm over all frequencies. However, finger length cannot increase indefinitely because it must be shorter than quarter wave length. Fig. 7(b) shows shorter finger length reduces the series resistance that eventually to the higher quality factor.

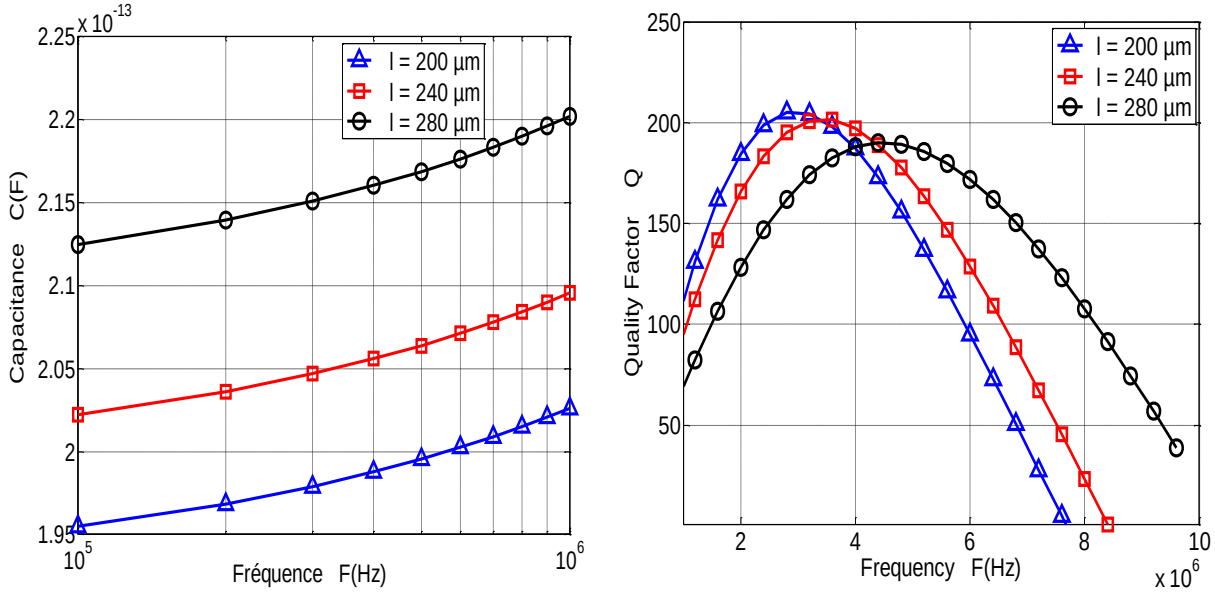

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Figure 7 Simulated results of the three different finger lengths, (a) Variation of the capacitance value with the frequency, (b) Variation of the quality factor with the frequency

2.4.Influence of the finger width

Different finger width give high impact to the capacitance curves, as shown in Fig. 8(a). Increasing the finger width will considerably increase the capacitance value, but the slope of the curves is almost similar. Fig. 8(b) show the effects of different finger width on quality factor as function of frequency. Higher finger width from 30 µm to 50 µm reduces the quality factor.

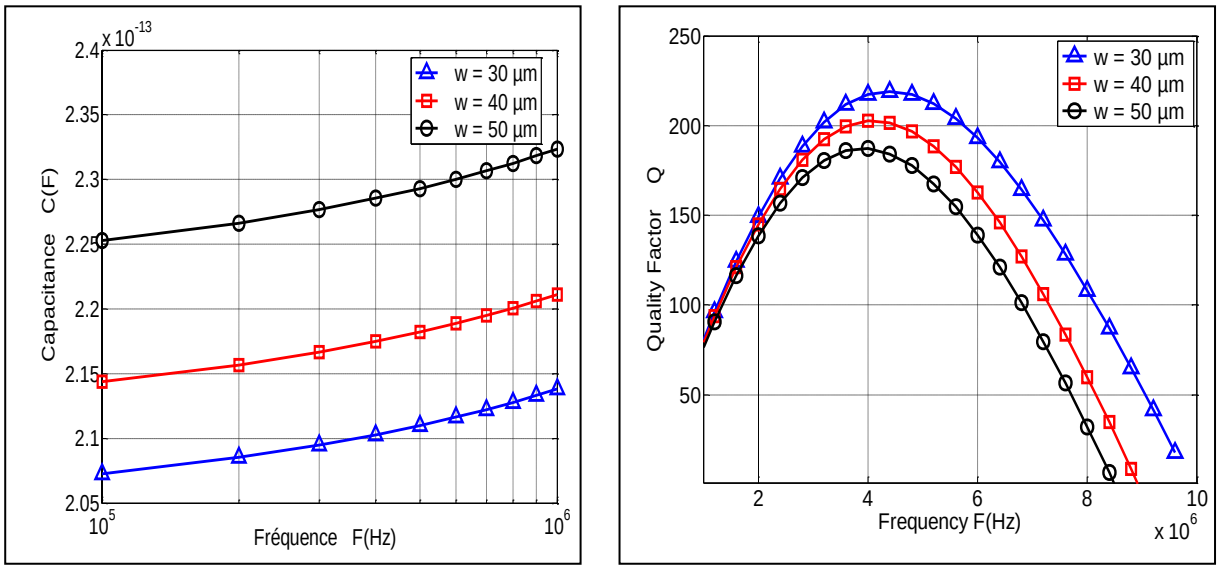

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Figure 7 Effect on (a) capacitance, (b) quality factor for different finger width of inter-digital capacitor

3. Buck converter applications

We have selected a Buck micro converter continuous-continuous step-down. The design specifications shown as Table 4:

Table 4: Design specification of buck micro converter

Parameter	Symbol	Value
Input Voltage	Vin	2,6 V
Maximum output voltage	Vout	0,8 V
Frequency of the converter	f	5 MHz

The simulation was executed using PSIM software 6.0. We achieved simulations in order to test the operation of our buck micro converter in two cases:

3.1.Converter including classical capacitor

The circuit of Fig. 9 contains a classical capacitor; Fig. 10 shows the waveform of the output voltage and current of the buck converter.

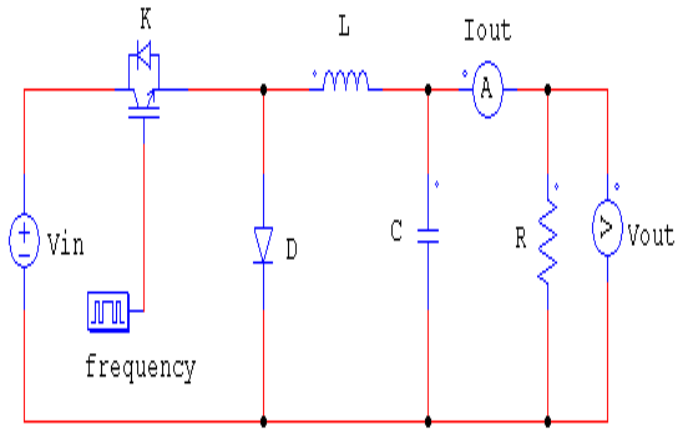

Figure 9 Buck converter with classic capacitor

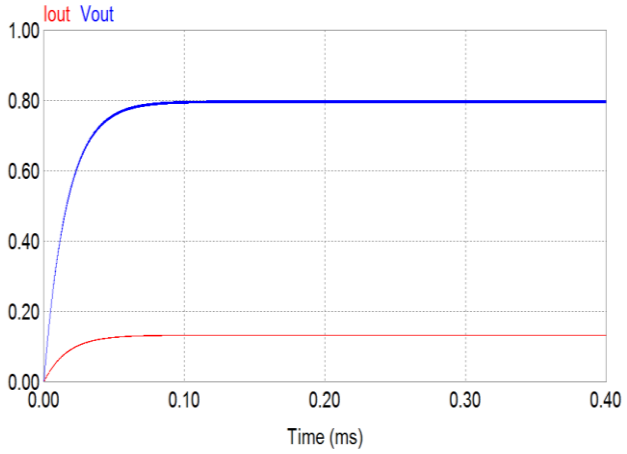

Figure 10 Output voltage and current of buck converter with classical capacitor

3.2.Converter including integrated inter-digital capacitor

Figure. 11 shows the change classical capacitor of buck converter by integrated inter-digital capacitor. The different electrical parameters of the equivalent electrical models are calculated in Table III. The simulated results are indicated in Figure. 12

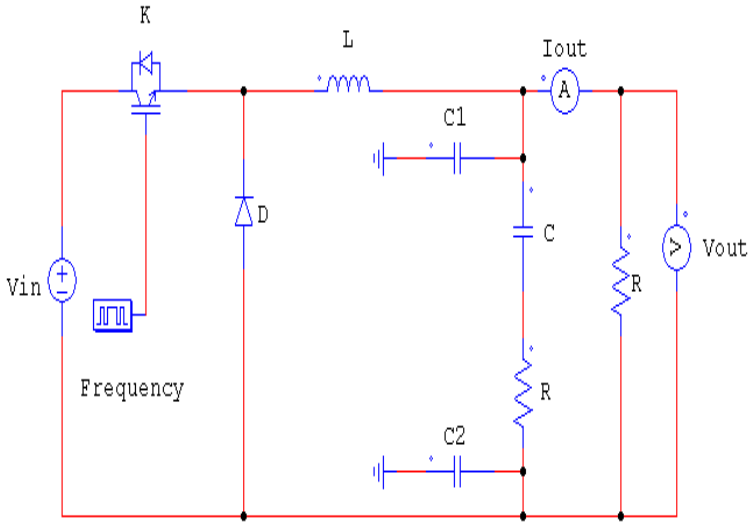

Figure 11 Buck converter with integrated inter-digital capacitor

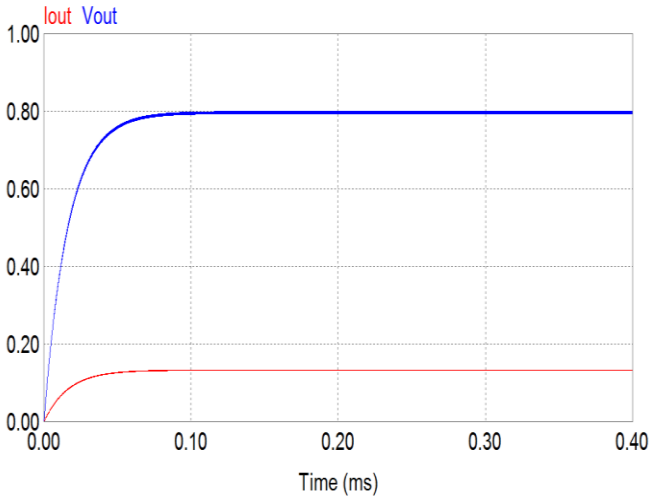

Figure 12 Output voltage and current of buck converter with integrated inter-digital capacitor

4. Conclusion

In this paper, we have presented the design and modeling of an inter-digital capacitor integrated of the substrate. The most difficult problem is to determine the geometrical and electrical parameters of the inter-digital capacitor. Next, the geometry of inter-digital capacitor is important and gives huge impact to the performance of RFIC. Indeed, the optimization of the quality factor of an inter-digital capacitor structure requires both weakly the finger width, finger length, number of finger and the spacing between fingers. Finally, by using a software simulation PSIM, we have compared the waveforms of the buck micro converter output voltages for the two simulations (classical capacitor, integrated inter-digital capacitor). We remark the same result between two cases.

5. References

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